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A Highly Efficient and Linear Class AB Power Amplifier for RFID Application

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Abstract

Power amplifiers (PAs) are usually the largest consumer of power in the transmitter. Therefore, designing a high efficiency RF power amplifier might be the best solution to cope with the problem of battery lifetime limitations in portable RFID code reader. In this paper, the designed circuit in Agilent ADS software is implemented using 0.18 µm RFCMOS technology at 3.3 v supply voltage. The measured results indicate that power added efficiency,out put power and power gain of the proposed class AB power amplifier at frequency of 2.4GHz are 35% , 30dBm and 28dBm.

Keywords*: Class AB, Linearity, PAE, Power Amplifier*

1. Introduction

RFID can provide automatic identification, tracking and management by radio frequency-based communication. RFID system is composed of two parts: transceivers and code reader. The main part of the RFID transmitter is linear power amplifier with high power. Since portable code readers are based on batteries, power amplifier consumes the largest part of power in code reader. So it is tried to have high efficiency. Moreover, linearity is one of the main parameters of power amplifiers (PAs). Class AB is widely used in wireless transceiver designs due to high linearity and high efficiency. In [1], a power amplifier composed of a parallel combination of amplifiers with Class A/AB led to improved linearity and increased power efficiency as well as reduced DC power consumption. In [2], the amplifier uses tuning technique in order to obtain the wide bandwidth and low power consumption, while it uses self-biased circuit to get high linearization. In [3], multi-band power amplifier uses a broadband matching network as a driver, while it uses reconfigurable matching network to increase the efficiency. In [4] and [5], the structure of CMOS power amplifier is constituted of input matching network, inter stage matching network, the output matching network, and a MOS switch- and varactor-based configurable tuning part .Uniformly coupled varactors with silicon on glass technology are used in order to implement tunable matching network, aiming at linearization improvement.

In [6] and [7], the memory polynomial digital pre-distortion (DPD) technique is utilized for linearizing of amplifiers. Exploiting Class F, inverse Class F, Class J or Class AB/I are proposed for boosting of efficiency. In [8], [9] and [10] Doherty method and Envelope Elimination and Restoration (EER) techniques are presented for high efficiency. A combined approach that includes a switchable matching network using diplexer concepts and load line regulation as well as transistor reconfigurable area techniques are presented in [11]. In [12], a multi-L section, a quarter-wavelength transfer, and cone transmission line transfer are proposed for broadband matching networks. In [13], designing a linear amplifier with transistor level compensation technique is used to increase linearization of CMOS power amplifier.

In this paper, first an overview of the proposed amplifier is presented and each block will be provided in detail. Then, the measured characteristics are shown at the 2400MHz frequency band.

2. Proposed Power Amplifier

In practice, the efficiency of the proposed Class AB power amplifier is about 25%. That is, power of 4W should be produced at an output power of 30dBm (1 W). In TSMC0.18µm

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technology, two types of transistors with voltage levels of 1.8 volts and 3.3 volts are available. Regarding the relationship between power and supply voltage, transistors with high breakdown voltage and voltage source of 3.3 V are used in this paper.

$$RL = \frac{1}{2}\frac{Vcc^2}{Ppeak} \quad (1)$$

Eq. (1) expresses equivalent resistance from transistor's drain in order for power supply. If one class is used for production of 4W, an approximate resistance of 10/8 will be required. Given that Q quantities for inductors are less than 10, thus equivalent resistance from drain should be considered much larger than inductors parasite resistance in order to reduce power losses and increase efficiency. Differential amplifier design has a wide variety of advantages in addition to power increase. Given the differential design and the use of four similar stages, the amount of resistance seen from drain is approximately R = 10. This might be favorable. Further, selection of more number of stages is not recommended as it leads to increased number of elements and lack of space. In this paper, in order to increase efficiency and gain, while maintaining linearization circuit, various techniques including differential, cascaded, multi-stage and matching circuits were utilized. Various techniques have been proposed in literature for linearization of power amplifier [1-13].

Due to high power of output and large number of elements used in this design, the use of linearization techniques, which use more elements beside the main amplifier, is not acceptable. In [1], by combining two linear and nonlinear classes, i.e. class A and B, one can make constant the final gm in a wide range of input. So the combination of linear and nonlinear classes not only leads to a high output power amplifier, but also results in appropriate linearization of final amplifier. Moreover, to combine these two linear and nonlinear classes, there is no need for additional elements. In this paper, a combination of two AB classes is used to improve linearization and high power. Given that the desired output power is high, application of linearization conditions only in the main power amplifier cannot respond to this wide range. So with the use of two different class AB power amplifiers, final linearization has been improved in the pre-amplifier.

Figure 1 and Figure 2 show schematic and layout representation of the proposed power amplifier circuit in detail. According to Figure1, the power amplifier consists of several main components: 1) Preamplifier 2) Main power amplifier 3) Power combiner using the transformer 4) The output matching circuit. All of the aforementioned components will be described further in detail.

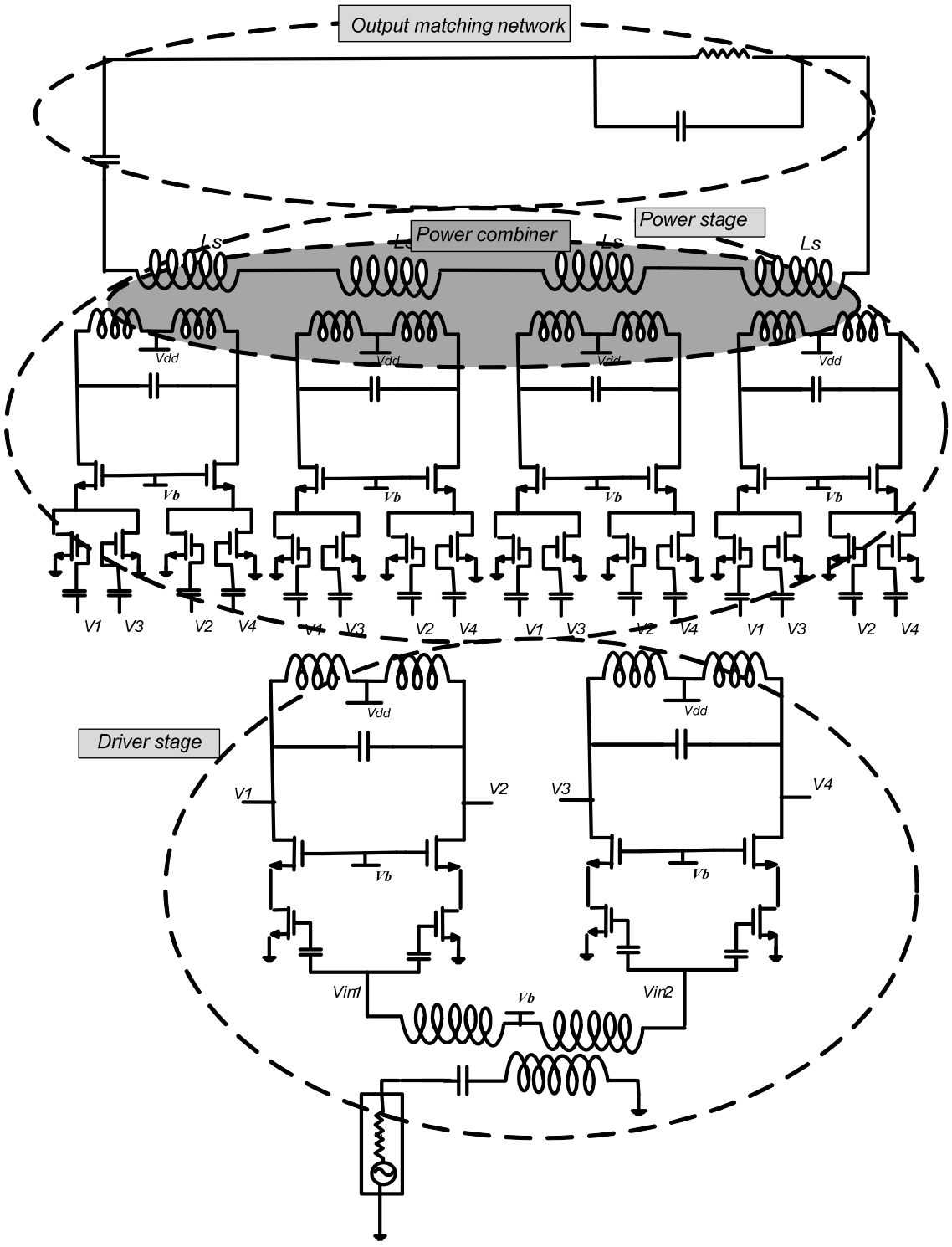

Figure 1. Illustrates schematic overview of the proposed power amplifier

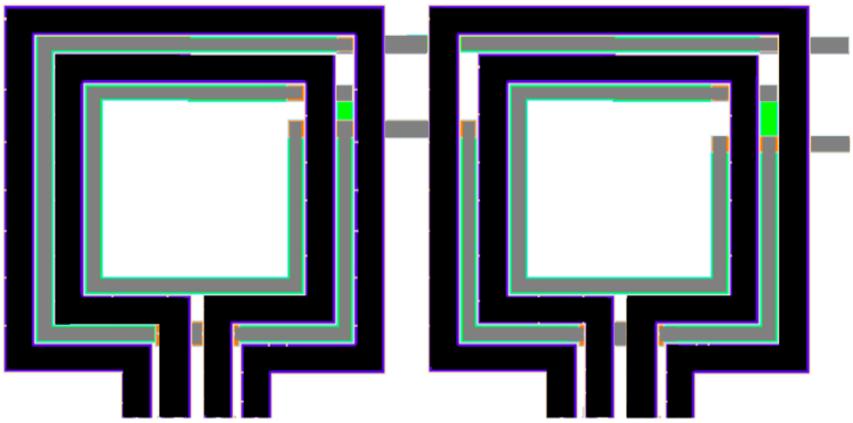

Figure 2. Layout of power amplifier

2.1. Preamplifier

The first stage is used as the driver in cascaded differential mode to match input bandwidth and high gain. The main task of the driver stage, indeed, is supplying the required voltage to drive the output stage. This means that driver stage considerably raises efficiency without much increase in power consumption. It should be noted that cascaded structure is preferred due to noticeable advantages such as increasing voltage level, the possibility of using higher supply than transistor breakdown voltage, providing maximum gain and output power, high reverse isolation between input and output, and increasing stability in high frequencies for power amplifier. Moreover, the differential structure is used because it may lead to even-order harmonics elimination and better stability against power supply noise, ground, and the substrate losses. Preamplifier stage is responsible for supplying a part of gain and consists of a single end transducer to differential and a filter at the load side. Stage of preamplifier is used with a combination method of transistors in a two-class differential cascaded structure in order to provide adequate gain and linearization in class AB, to put the transistors at the input of amplifier in class AB, we used the proper bias. Operating point matching is performed by changing the gate voltage. This part also has a key role in the operation of the circuit.

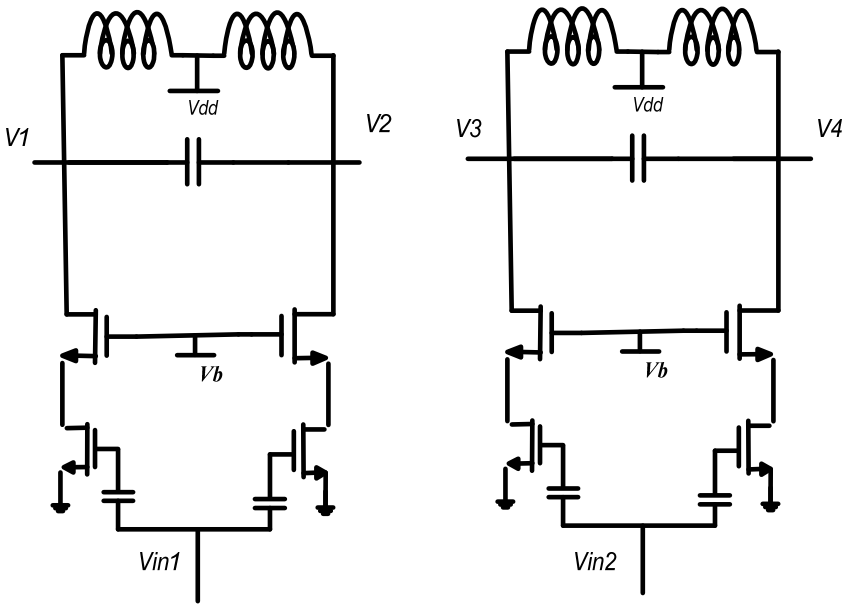

Figure 3. Preamplifier circuit

2.2. Main Amplifier

Figure 4 shows the main amplifier circuit in which the differential structure and parallel transistors are used to enhance the current flow, linearization, and maximum power. This stage is, indeed, the main supplier of the gain.

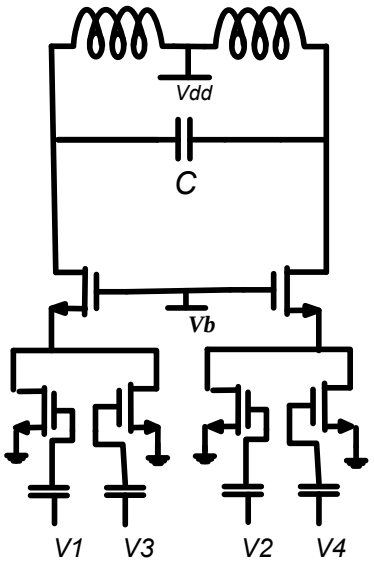

Figure 4. Main part of dual band class AB amplifier

2.3. Power Combiner Circuit

So in this paper, power combiners are used in two stages to produce an output power. The first combiner in the main amplifier accomplishes both combination and linearization tasks, while the second combiner uses the transformer, which is connected as the main amplifier and adds power of amplifiers together. In order to produce high powers with low power elements, various circuit techniques are available that can be divided into two combined series and parallel categories. In series technique, by putting together the low voltage elements a larger voltage supply can be achieved and high power is produced. Whereas in parallel mode, high power can be achieved through the combined smaller powers [14]. Because of the low power consumption in this paper, the series method cannot be used. In this paper, 4 transformers are needed for 4 stages. Considering the low operating frequency, the size of transformers on chip occupies a large space. Therefore, the trans-intensive method is used for implementation.

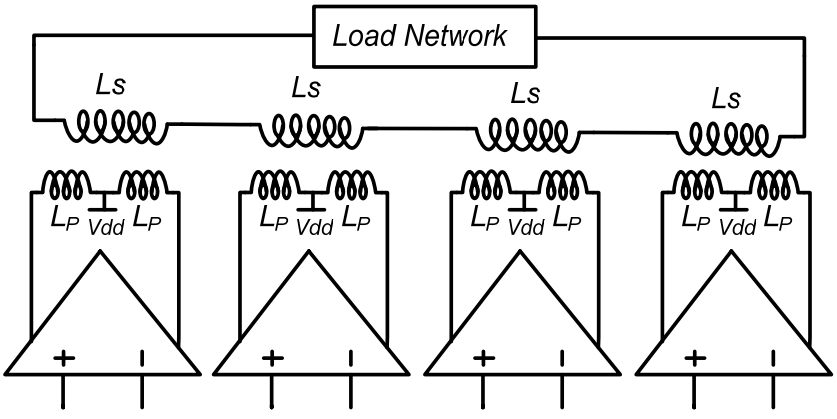

Figure 5. Power combiner

2.4. The Output Matching Circuit

The output matching circuit is challenging issues in the design which leads to the maximum power transfer. The output matching circuit transfers the maximum power to the load. Matching circuits are tuned for 2.4GHz frequency.

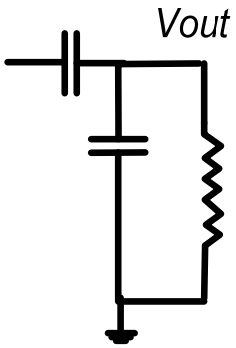

Figure 6. Filter of output stage

5. Simulation Results

In this paper, simulations were carried out on Agilent ADS software. In order to perform simulations, first the combination circuit should be optimized. Based on the optimization methods and MATLAB software, optimal values were obtained. Then, the parameters of transformers were extracted in Momentum ADS Agilent. Afterwards, by using the matching circuit, the equivalent circuit of the transformer was obtained as inductor and capacitor. Due to the large parasitic elements that exist in the circuit, the exact calculation of the elements manually is very difficult and complex. First, elements are approximately calculated. Then, they are obtained by optimization method in ADS Agilent. Repeating the optimization process several times will result in desired solution at 2.4GHz frequency. Priorities of optimization are output power, efficiency, observing the breakdown voltage of transistors, and linearity of amplifier with consideration of IM3 and IM5.

5.1. Simulation Results for Frequency of 2.4GHz

Figure 7 shows output power, efficiency, and gain of power amplifier at the frequency of 900MHz. Output power at 1dB, efficiency, and gain at frequency of 2.4GHz are approximately 30dBm, 35%, and 28dBm respectively. In Figure 8, IMD3 and IMD5 values are calculated by application of two tunes.

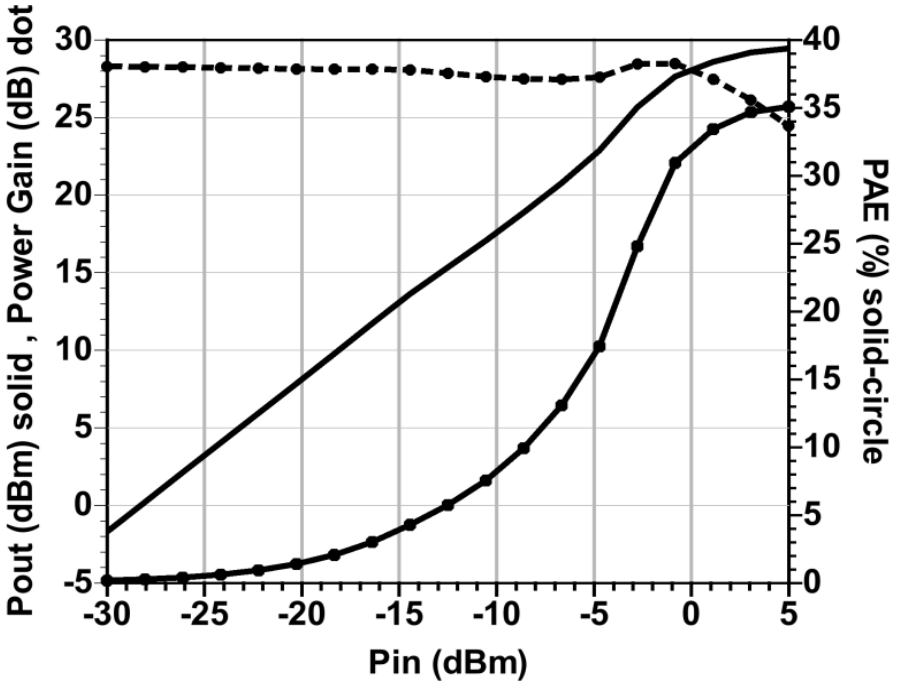

Figure 7. Illustrates curves related to efficiency, gain, and measured output power at the frequency of 2.4GHz.

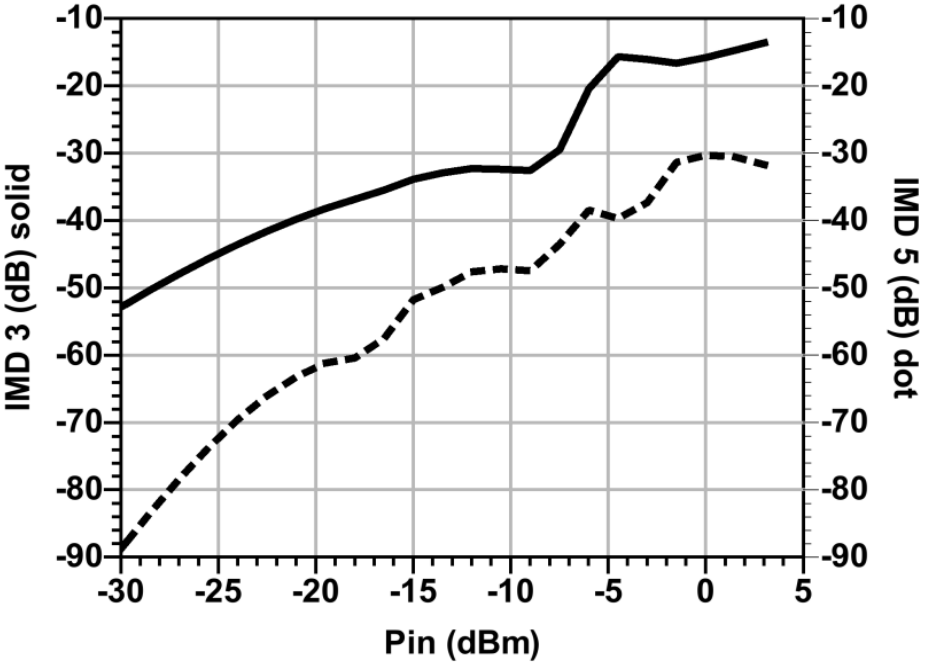

Figure 8. Curves of IMD3 and IMD5 in terms of input power at the frequency of 2.4GHz.

6. Conclusion

In this paper, a class AB power amplifier is designed for MHz 2.4GHz with issues such as circuit schematics, circuit function and the design process is discussed. Class AB operation provides the opportunity to balance the tradeoff between linearity and efficiency. The proposed structure consists of a preamplifier, main circuit, power combiners, and output filter. Finding a structure with optimized efficiency, 2.4GHz frequency .The circuit designed in ADS 2011

software is implemented with 0.18 µm CMOS technology proper output power and linearity for PA is the goal of this paper owing to the fact that, PA consumes the most amount of power from the supply/battery.The proposed circuit provides 30dbm output power, 35% of efficiency.

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